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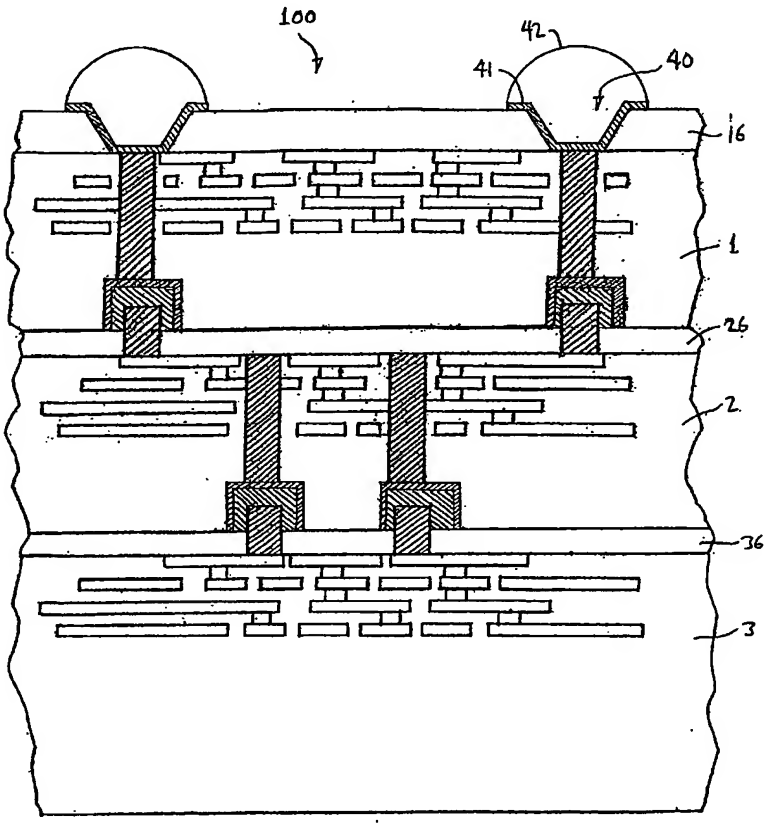
(54) Title: THREE-DIMENSIONAL DEVICE FABRICATION METHOD



(57) Abstract: A method is described for fabricating a three-dimensional integrated device including a plurality of vertically stacked and interconnected wafers. Wafers (1, 2, 3) are bonded together using bonding layers (26, 36) of thermoplastic material such as polyimide; electrical connections are realized by vias (12, 22) in the wafers connected to studs (27, 37). The studs connect to openings (13, 23) having a lateral dimension larger than that of the vias at the front surfaces of the wafers. Furthermore, the vias in the respective wafers need not extend vertically from the front surface to the back surface of the wafers. A conducting body (102), provided in the wafer beneath the device region and extending laterally, may connect the via with the matallized opening (103) in the back surface. Accordingly, the conducting path through the wafer may be led underneath the devices thereof. Additional connections may be made between openings (113) and studs (127) to form vertical heat conduction pathways between the wafers.

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TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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